A Low-Power Direct Conversion Receiver Module for C-Band Wireless Applications

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Abstract — **In this paper, we present the first low-power direct conversion receiver module for broadband wireless applications at C-band. This module is composed of a highly-integrated receiver MMIC fabricated in a 0.6 μm commercial GaAs MESFET process mounted on a LTCC substrate with an integrated multi-layer three-dimensional front-end filter. With only 25 mW of dc power consumption, this receiver module demonstrates a conversion gain of 9 dB, NF of 4.7 dB, dc offset below –70 dBm, IIP2 of +30 dBm, and IIP3 of -10 dBm at 5.8 GHz.**

I. Introduction

Increasing demand for wireless audio, video and data services has triggered significant activities in deployment of broadband wireless systems in the C-band frequencies. However, this growth has been challenged by the lack of cost-effective and highly integrated microwave components. In such scenario, alternative topologies such as direct conversion and integration of appropriate fabrication processes can help to overcome the challenges of typical heterodyne topologies and reduce the cost of the transceiver. A variety of direct conversion receivers have been implemented in both GaAs and Si, but these receivers mostly present an incomplete solution or a compromise between performance and integration [1-3].

In this paper, we present an integrated low-power direct conversion receiver module that optimizes cost and performance by utilizing a commercial semiconductor process and a multi-layer ceramic package. As shown in Fig. 1, this module consists of a direct conversion GaAs IC integrated with a ceramic front-end filter. This filter is fabricated in a high-volume low-temperature co-fired ceramic (LTCC) process. Using this multi-layer LTCC process, high Q and compact ceramic passives, transmission lines, and filters are fabricated with relative ease and great repeatability. By using direct conversion, the concern for the image frequency is eliminated, and a LTCC filter can be used for sufficient rejection of the out-of-band blockers.

Using a commercial GaAs Metal-Semiconductor FET (MESFET), we previously demonstrated the first compact C-band direct conversion receiver microwave monolithic integrated circuit (MMIC) [4]. In this paper, we introduce a new low-power MMIC integrated with a three-dimensional LTCC front-end filter. The receiver MMIC occupies 75x60 mil^2 of die area and consumes only 25 mW of dc power from a 3 volt supply. The LTCC filter occupies 5.6 mm x 3.1 mm x 2.2 mm and provides 1.8 dB of insertion loss with greater than 10 dB of rejection at 220 MHz offset.

II. Module Design

The block diagram of the receiver module is shown in Fig.1. This module consists of a LTCC front-end filter directly wirebonded to a direct conversion receiver MMIC.

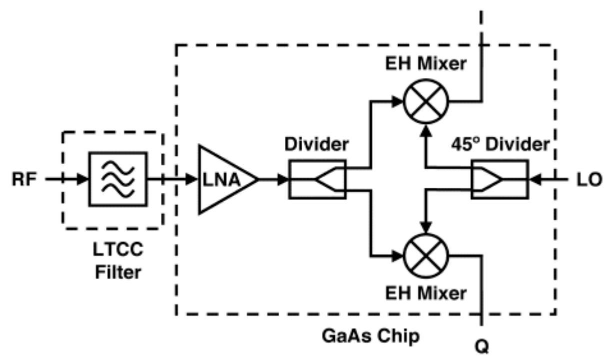

Fig. 1. Block diagram of the receiver MMIC.

A. Integrated LTCC Bandpass Filter

An integrated front-end band pass filter, first demonstrated in [5], has been, designed, fabricated and measured as part of the entire receiver in a commercial multi-layer LTCC technology utilizing ten 4.4 mil thick 943AT ceramic tapes. To maintain the compactness of the module, the filter was designed using a folded coupled-stripline (FCL) configuration whose diagram is illustrated in Fig. 2. This is based on a conventional edge-coupled-line band pass filter except the coupled line segments were deployed vertically on different layers. The availability of a multi-level dielectric system allows the realization of the multi layer version of the edge-coupled line filter. The bottom portion of Fig. 2 shows the cross sectional view of this FCL filter, showing two vertically deployed coupled line segments of the filter. The two via-connected segments are separated by a middle solid metalization, which acts as the top and bottom stripline grounds for the bottom and the top segments, respectively. The three ground stripline ground planes are physically connected by vias. To allow on-wafer characterization using air coplanar probes, the input and output have to be on the same layer which requires a good stripline to coplanar waveguide transition. The actual input and output, however, can be connected to the antenna's vertical feed through the top most ground plane and to the rest of the modules deployed in the bottom layers through the bottom most ground plane.

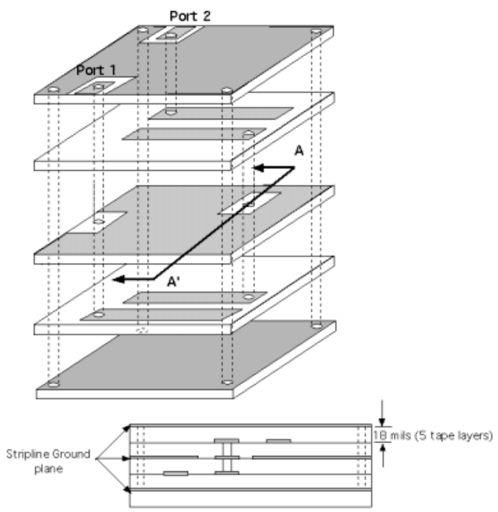

Fig. 2 A three-dimensional view of a folded coupled line filter (top) and a cross-sectional view on AA' (bottom).

The photograph of the first FCL filter prototype whose total size is 5.6 mm x 3.1 mm x 2.2 mm with CPW pads is shown in Fig. 3. Figure 4 shows its measured results demonstrating 15 dB of return loss and less than 1.8 dB of insertion loss at the center frequency of 5.6 GHz. In addition the filter demonstrated a measured narrow band performance of about 200 MHz and therefore, the Q factor is about 28. The center frequency experienced a shift from 5.8 to 5.6 GHz because of the additional inductive and capacitive parasitic caused by the vias. These are the vias interconnecting the stacked coupled-line segments, as well as the vias connecting the input and output of the filters to the MMIC chips attached on the surface of the LTCC substrate. A design rule predicting the effects of the inter-segment vias, including the effects of vertical stripline to coplanar waveguide transition, has been developed for future filter design and development.

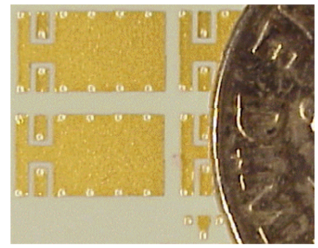

Fig. 3 Photograph of the C-band folded coupled line filter

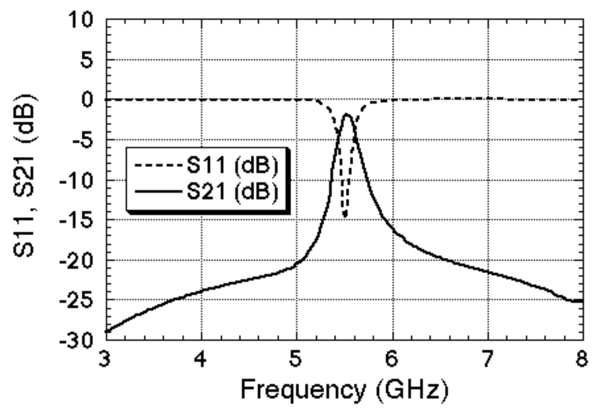

Fig. 4 Measured results of the LTCC-integrated folded coupled line filter.

B. Receiver MMIC

The MMIC is composed of a high-linearity low-power LNA followed by a Wilkinson power divider, and two even-harmonic mixers. The LO is supplied to the mixers by a modified Wilkinson power divider that incorporates a 45˚ phase shift in one of the LO paths. Because of the doubling action in the mixers, only 45˚ of phase-shift is required to produce in-phase (I) and quadrature-phase (Q) signals at the mixer output. Figure 5 shows the circuit schematic of the receiver MMIC.

The LNA is composed of a 400-µm common source FET followed by two 300-µm FETs in a cascode configuration [6]. This LNA has a gain of 24 dB, IIP3 of –12 dBm, and NF of 2.3 dB with 6 mA of dc current. All enhancement-mode devices are used to simplify dc biasing with positive supply voltages. The LNA feeds the RF signal into the even-harmonic mixers through a Wilkinson power divider. Each mixer is composed of a pair of 300-um resistive FETs that are pumped by the LO signal at the gate through a spiral coupled-line transformer. This type of transformer provides great performance with small size implementation [7]. A resonant tank made up of a metalinsulator-metal (MIM) capacitor and a spiral inductor is used in this mixer to isolate the RF and IF port at the drain of the FETs. By using this even-harmonic mixer topology we are able to increase IIP2, alleviate in-band LO leakage and reduce the time-variant dc offset [4,8]. Because of the frequency scheme of such mixers a LO frequency of 2.9 GHz is used to down-convert the RF band of interest at 5.9 GHz. Mixers show a loss of 9 dB, IIP3 of +15 dBm, and IIP2 of above +30 dBm with a LO power of 12 dBm.

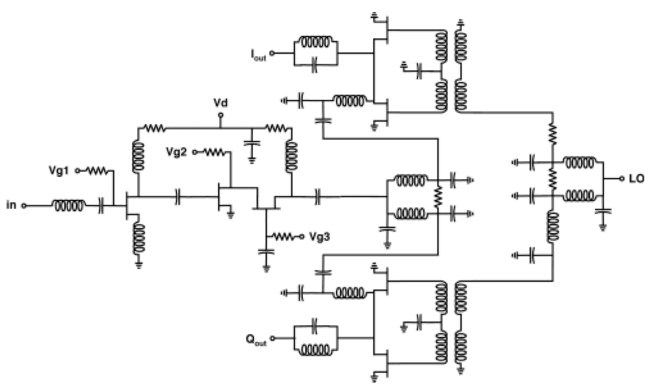

Fig. 5. Circuit schematic of the receiver MMIC.

As shown in Fig. 6, all receiver blocks are integrated together on a 75x60 mil^2 die area. The overall performance of the receiver is shown in Table I. The receiver demonstrates excellent NF, linearity, and rejection of out-of-band blockers with only 25 mW of dc power dissipation.

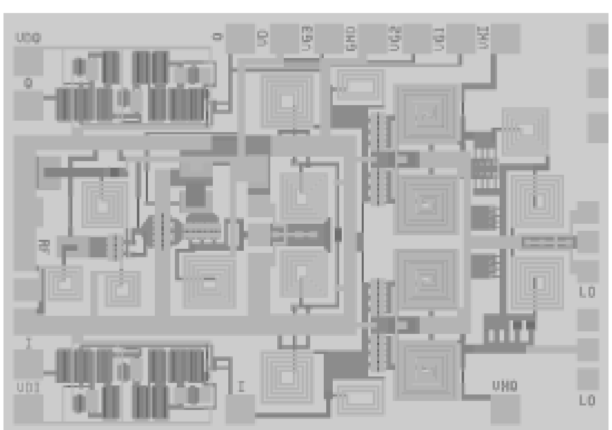

Fig. 6. Picture of the receiver MMIC.

TABLE I

RECEIVER CHARACTERISTICS

Gain	9 dB
NF	4.7 dB
Dc offset	-70 dBm
IIP3	-10 dBm
IIP2	+30 dBm
Current	7 mA
S11	-10 dB
Blockers	-10 dB @ ±220 MHz

IV. CONCLUSION

A low-power direct conversion receiver module for broadband wireless applications at C-band has been demonstrated. This module that consist of a three-dimensional LTCC filter and a highly integrated low-power MMIC, shows excellent performance and a compact implementation. With only 25 mW of dc power consumption, this receiver module demonstrates a conversion gain of 9 dB, NF of 4.7 dB, dc offset below –70 dBm, IIP2 of +30 dBm, and IIP3 of -10 dBm at 5.8 GHz.

ACKNOWLEDGEMENT

The authors wish to acknowledge TriQuint Semiconductor, Yamacraw Design Center, Georgia Tech Packaging Research Center, and Ray Brown and Mike Ehlert of National Semiconductor for their support of this work.

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